REMARKS/ARGUMENTS

Claims 9-26 are currently pending. Claims 9-24 stand rejected. By this amendment, claims 9, and 16 are amended, and claims 25 and 26 are added. Claims 9-24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hirano (U.S. Patent No. 5,650,742) ("Hirano") in view of Cress et al. (U.S. Patent No. 6,483,386) ("Cress").

Claims 9 – 16 Amended, 25, 26 Added, Reciting "a gate that is grounded"

Claims 9 and 16 have been amended to recite "at least one native NMOS transistor device having a threshold voltage less than 0V and a gate that is grounded", among other limitations. Claims 25 and 26 recite "at least one native NMOS transistor device" having "a gate that is grounded", among other limitations.

It is respectfully submitted that neither Hirano or Kress teach or fairly suggest a "native NMOS transistor device" with "a gate that is grounded". Examiner has indicated that "Figure 1,31 of the Hirano reference discloses a level shifter circuit (101, 3001), which meets a method of translating a voltage level of a single-ended input signal (I1) using at least one pass NMOS transistor device (Qn101, Qn3001)...".

Although the foregoing statement is disagreed with, it is submitted, at the very least, that Hirano Figures 1, and 31 clearly does not teach "at least one native NMOS transistor device having a threshold voltage less than 0V and a gate that is grounded." In contrast, Hirano teaches at Col. 1, Lines 26-27, that a "gate of the N-channel MOS transistor Qn3001 is connected to the first voltage source VCC...". Additionally, Hirano teaches at Col. 7, Lines 6-7, that "a gate of the N-channel MOS transistor Qn101 is connected to the input signal S1."

Examiner has indicated that the "Cress, et. al. reference discloses (note M3 in Figure 5, lines 45-65 of Col. 2, lines 18-43 of Col. 3, and lines 4-31 of Col. 4 of Cress, et. al.) a pass transistor device (M3) is a native NMOS transistor device having a threshold voltage less than 0V...".

Although the foregoing statement is disagreed with, it is submitted, at the very least, that Cress clearly does not teach "at least one native NMOS transistor device having a threshold voltage less than 0V and a gate that is grounded." In contrast, Cress teaches at Col. 3, Lines 26-29 that "the gate of the native device M3 is controlled by a signal (e.g., LV_COMP_EN) whose high level does not exceed the internal regulated supply."

For at least the foregoing reasons, Examiner is requested to withdraw the rejection to claims 9, 16, as well as dependent claims 10-15, and 17-19, and allow claims 25 and 26.

Claim 20, Neither Hirano Figures 1 or 31 teach "single ended input" AND "eliminating static current drain"

Claim 20 recites, among other limitations, a "level shifter circuit having a single ended input" and "eliminating static current drain".

Examiner has indicated that "Figure 1,31 of the Hirano reference discloses a level shifter circuit (101, 3001), which meets a method of translating a voltage level of a single-ended input signal (I1)" and Hirano teaches "eliminating static current drain (by feed back transistor Qp101 in Figure 1, or Qp3001 in Figure 31)." The foregoing rejection is traversed because neither Hirano, Figure 1 or Hirano, Figure 31 teach "single ended input" and "eliminating static current drain."

Hirano Figure 1 does not teach the claimed "single ended input".

Examiner has indicated, "Note that the signal S1 is a control signal for the circuit, not an input signal, i.e., the circuit 101 in Figure 1 receives only one input

data signal (namely I1), and the signal S1 is the control signal to control transistor Qn101 of the circuitry." Applicants respectfully traverse and submit that "In Figs. 1 and 8, I1 and S1 indicate input signals." Hirano, Col. 6 Lines 49-50. (Emphasis Added) See also, Col. 7, Lines 6-7 and Col. 8, Lines 21-22. Therefore, the level shifter circuit 101 in Hirano, Figure 1, does not teach "having a single ended input.

Accordingly, it is requested that the rejection to claim 20 under 35 U.S.C. 103(a) from Hirano, Figure 1 in view of Cress be withdrawn.

Hirano Figure 31 does not teach "eliminating static current drain".

Examiner has indicated that Hirano teaches "eliminating static current drain (by feed back transistor Qp101 in Figure 1, or Qp3001 in Figure 31)." The foregoing statement as it relates to Hirano, Figure 31 is traversed. The foregoing statement as it pertains to Hirano, Figure 1 is moot in view of the above reasoning, and will not be addressed.

Although Examiner has made reference to "Qp3001 in Figure 31" Hirano does not indicate (and Examiner has not cited) anywhere that "Qp3001" causes "eliminating static current drain". Moreover, Hirano states that "a through current flows from the second voltage source VPP to the ground voltage source VXX via the N-channel MOS transistor Qn3002 and the P-channel MPS transistor Qp3002 which causes a disadvantage that the voltage level of the output signal O30 cannot fixed at the "L" level." Hirano, Col. 2, Lines 27-32.

Therefore, Hirano, Figure 31 does not teach or fairly suggest "eliminating static current drain." Accordingly, it is requested that the rejection to claim 20 under 35 U.S.C. 103(a) from Hirano, Figure 1 in view of Cress be withdrawn.

CONCLUSION

In view of the foregoing, it is respectfully submitted that the pending claims define allowable subject matter. Applicants respectfully request that the present case pass to allowance. Should anything remain in order to place the present application in condition for allowance, the Examiner is kindly invited to contact the undersigned at the telephone number listed below.

Please charge any required fees not paid herewith or credit any overpayment to the Deposit Account of McAndrews, Held & Malloy, Ltd., Account No. 13-0017.

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Respectfully submitted,

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